EDA for Multi-die System Integration in a Package

Exploration ➔ Design ➔ Optimization ➔ Validation ➔ Analysis ➔ Signoff

Rita Horner
Sr. Product Marketing Manager, 3DIC Compiler
September 2020
Multi-Die Advanced Packaging
Bandwidth, Performance, Power, Latency, and Development Cycle

Cost of Advanced Designs ($M)

- IP Qualification
- Architecture
- Verification
- Physical
- Prototype
- Validation

Source: Design Activities and Strategic Implications, IBS 2019

Wafer and reticle size
Max. Stepper ~800 mm²
(not to scale)

Signal/Power Thermal Integrity Designers
SoC Designer
System Architect
PCB Designer
Package Designer
Printed Circuit Board (PCB)
Example Die-to-Die Physical Interfaces (PHYs)

High Bandwidth Memory/Interconnect (HBM/HBI), Ultra/Extra Short Reach (USR/XSR)
# Die-to-Die PHY Options in Advanced Process Nodes

## Parallel vs. Serial Interfaces

<table>
<thead>
<tr>
<th>Standards &amp; Specifications</th>
<th>Parallel Interface</th>
<th></th>
<th>Serial Interface (SerDes)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non-Memory</td>
<td>DARPA, OCP-ODSA AIB, HBI, BoW</td>
<td>JEDEC HBM2, HBM2E HBM3</td>
<td>IEEE 802.3, PCI-SIG, OIF 1G - 56G &amp; 112G URS/XSR</td>
</tr>
<tr>
<td>Memory</td>
<td>1 to 2 → 2 to 4 → 4 to 6</td>
<td>2.4 → 3.2 to 3.6 → 6.4</td>
<td>1.25 to 112</td>
</tr>
<tr>
<td>Data Rate per Lane (Gbps)</td>
<td>30 to 2000+</td>
<td>1024</td>
<td>2 pairs (4) ✓</td>
</tr>
<tr>
<td>I/O number per link</td>
<td>Low ✓</td>
<td>Low ✓</td>
<td>High</td>
</tr>
<tr>
<td>Latency</td>
<td>Short</td>
<td>Short</td>
<td>Long ✓</td>
</tr>
<tr>
<td>Interconnect reach</td>
<td>High density routing (Silicon Interposer)</td>
<td>Low resistance (High Density Fan-Out)</td>
<td></td>
</tr>
</tbody>
</table>
IC Packaging “Adjacency” Rapidly Morphing into Core EDA

- Low density routing
- Large width & spacing
- Design driven manufacturing
- Non-Manhattan shapes

**OSATs & Substrate Manufacturers**

**Silicon Foundries**
- High density routing
- Small width & spacing
- Manufacturing drives design (PDKs)
- Manhattan based shapes

**Silicon Interposer**

**Silicon/Glass Interposers**

**package Substrate Design Rules**

- Line/Space (L/S)
  - 100 µm
  - 10 µm
  - 0.1 µm
  - 100 nm
  - 10 nm
# Advanced Packaging Technologies

Interconnect Density, Trace Length, Performance, Size and Cost

<table>
<thead>
<tr>
<th></th>
<th>Routing Density w/s</th>
<th>Trace length</th>
<th>Trace loss</th>
<th>Size</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-Chip-Module (MCM)</td>
<td>Low</td>
<td>Long</td>
<td>Low</td>
<td>Large</td>
<td>Low to Med</td>
</tr>
<tr>
<td>Organic built-up</td>
<td>≥ 8 μm width &amp; spacing</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wafer level Fan-Out</td>
<td>Med. to High</td>
<td>Med. to Long</td>
<td>Med. to Low</td>
<td>Medium</td>
<td>Med. to Low</td>
</tr>
<tr>
<td>Re-distribution layer (RDL)</td>
<td>≥ 2 μm</td>
<td>Long</td>
<td>Low</td>
<td>Medium &gt; 2x reticle</td>
<td>Low</td>
</tr>
<tr>
<td>Silicon /Glass Interposer</td>
<td>High</td>
<td>Short</td>
<td>High</td>
<td>Small 2x reticle</td>
<td>High</td>
</tr>
<tr>
<td>Through silicon Via (TSV)</td>
<td>~ 0.4 μm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Diagram:
- Multi-Chip-Module (MCM)
- Organic built-up
- Re-distribution layer (RDL)
- Silicon /Glass Interposer
- Through silicon Via (TSV)
2.5D/3DIC Design Challenges
Signal Quality, Power, Thermal & Mechanical Stress

- Signal integrity
- Power integrity
- Thermal integrity
- Mechanical stress
- Complex physical verification and analysis

Chip-Package Co-Design for an Optimal Solution!
# Multi-Die Package Design EDA Tools Today

## Existing Limitations and Challenges

- Disjointed solutions with multiple point tools,
  - Limited cross-discipline collaboration support
  - Each with own interfaces and use models
  - Large feedback loops for convergence
  - Lack of automation
  - Separate use models
  - Database size limitations

- Power/signal/thermal noise optimization starts too late in the design cycle

- Multiple point tools each w/ separate capability and scripts. Lack support for early exploration and end to end validation

## Multi-Die Integration Solution

- A unified platform that enables cross-discipline co-design & co-optimization
  - Unified GUI interface, 3D & 2D view
  - DRC-aware environment
  - Automation (routing/shielding, bump placement, …)
  - Common data model, enabling scalability in capacity and performance

- Power/signal/thermal noise aware design optimization from early exploration to design signoff (die to PCB)

- SoC-scale integrated platform from early architectural exploration, to design/implementation, validation, to signoff
Ideal Multi-Die Design Platform for a System in a Package
Auto-Routing & Auto-Shielding

Fan-Out routing (any-angle, teardrops & oblong shapes, degassing hole)

HBM Signal Automatic Routing & Shielding

45 & 90 Degree Routing & Shielding

Si Interposer
Multi-Die System Integration – Analysis & Validation

Signal Integrity, Power Integrity, Thermal/Mechanical Integrity, DFT Rule Check → Signoff

**Extraction & Signal Integrity**

**DFT Rule Check**

Logical and physical connectivity check

**Sign-Off (STA, DRC/VS)**

Output from Project Moore

- Die 1 Verilog
- Die N Verilog
- Die 1 SDF
- Die N SDF

**PrimeTime**

- Top-Level Netlist
- Top-Level SDC
- Constraints
- Advanced Packaging
- Verilog Netlist, SPEF

**IC Validator**

- DRC/LVS on Die-die Interface

**EM/IR & Power Analysis**

**Thermal & Mechanical Analysis**

Thermal hotspot detection & correction
Temperature aware resistance, EM, IR

**Physical Verification**

Misalignment
Thank You