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AT&T
XGS-PON 1RU vOLT

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1RU vOLT

- General Info
  - Dimensions
  - Environmental compliance
  - Power Supply & Fans redundancy

- Main blocks
  - PON
  - QAX - Switching & TM device
  - CPU Device
  - Control FPGA
  - Timing Block
  - PCIe Switch

- vOLT Box PON links options
  - High Density 1RU Option 1 - 16x XGS-PON/NGPON2 links with uplink in the front

- Traffic and BW modes
- Estimated Power budget
1RU vOLT General Information

The system is a physical 1RU vOLT that is self-contained, and not part of a physical chassis system. However, this box can also be considered a line card in a virtual, scale-out system where such line cards are attached to a switch fabric.

- **Environmental compliance**
  - See OCP Submittal Document Appendix A

- **Dimensions**
  - 1RU design that supports standard 19" rack deployments as well as standard 21" Open Rack and also 23" telco rack deployments.

- **Power Supply & Fans redundancy**
  - Redundant field replaceable (hotswappable) power supply and fan units
    - Power supply optional PN: Delta DPS460KBD/BE
    - Fan optional PN: Delta, GFCB0412EHS-D

<table>
<thead>
<tr>
<th></th>
<th>Inches</th>
<th>Millimeters</th>
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<tbody>
<tr>
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<td>520</td>
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<tr>
<td>Width</td>
<td>17.08</td>
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<tr>
<td>Height</td>
<td>1.73</td>
<td>44</td>
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*Note: Width does not include mounting ears. Depth does not include PSU handles.*
Main blocks

- **PON**
  - 16 ports x 10/10 XGS-PON (XFP) using the Mable (BCM68258) Chip

- **QAX** - Switching & TM device
  - Supports up to 300GB traffic (meets all flexible vOLT various link requirements)
  - Requires total of only 6x DDR4 devices
  - Uplink NNI – using 2x2 QSFP28 – already taking in considerations the uplink redundancy needs

- **CPU**
  - Using BRCM XLP208 chip
  - Memory: DRAM - 2GByte DDR3 72bit, NAND Flash + SDIO
  - Management: PCIe gen 2.0 + SPI

- **Control FPGA**
  - Serves for general ‘glue logic’ applications
    - For example: I2C control, LEDs, Interrupts + I/O expander, Fan and PS control, Power sequencing,
  - FPGA device (example PN): XC3S700AN-4FGG484C

- **Timing Block**
  - System clock driver (provides all reference clocks to all blocks) - Supporting 8KHz, Sync-E, 1588, Amd.2 and 1PPS options
  - Using Microsemi ZL30143

- **PCIe Switch**
  - To allow PCIe management of all main devices on-board (Maple devices + QAX)
1RU vOLT 16x XGS-PON links

- **PON Links**
  - Using 8x Maple (BCM68628) blocks
  - 16x XGS-PON links
  - Optics form factor – XFP

- **NNI Links**
  - NNI – using 2x2 QSFP28
  - Located on the front panel
1 RU vOLT 16x XFP links

- Front Panel Includes
  - 16x XFP form factor xPON links
    - XGS-PON or NGPON2 or XGPON1
  - NNI Uplink – using 4x QSFP28 (supporting redundancy)
  - User ports – 2x RJ45 stacked

425 mm
3D simulation - 16x XFP links

- 1RU vOLT