ODSA
Enabling Heterogenous Integration

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ODSA Workgroup

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ASE Introduction
Organization

ASE Technology Holding, Co.

ASE
IC Assembly, Test & Materials
Est. 1984

SPIL
IC Assembly / Test
Est. 1984

USI
ODM / DMS / EMS
Est. 1976

2019 Revenue: $8.13B
2019 Revenue: $5.37B
Providing Complete Value Chain Solution

Integrating OSAT and EMS

ASE Group Services
Packaging Market Drivers
Semiconductor Revenue vs. Process Generation

Impact of Moore slowing?
Value of Semiconductor Packaging is Increasing

Technology Node vs Packaging Revenue US $

- 1970: 500 um
- 1980: 250 um
- 1990: 100 um
- 2000: 50 um
- 2010: 10 um
- 2020: 5 um
- 2030: 3 nm

CMOS: 90 nm

PCB/Substrate: 10 um

Value of Packaging: 1600 X

Packaging Revenue US $
- 10 B
- 20 B
- 30 B
- 40 B
- 50 B
- 60 B
Chip & System Integration Convergence

- **Technology Node**
  - 10 um
  - 3 um
  - 1 um
  - 0.8 um
  - 0.35 um
  - 90 nm
  - 28 nm
  - 16 nm
  - 7 nm
  - 3 nm

- **Complexity**
  - 1970
  - 1980
  - 1990
  - 2000
  - 2010
  - 2020
  - 2030

- **Package Integration**
  - DIP
  - QFP
  - BGA
  - FC BGA
  - SiP

- **SOC: Chip Integration**

- **System Integration**

- **Heterogeneous Integration**
Silicon Integration Packaging Solutions
Silicon Integration Solutions

SiP
- PCB/Substrate interconnect
- Low/med density D2D
- > 25um line/space
- > 200um bump pitch
- > 50um comp spacing
- Bare/packaged parts
- Chip last process

Flip Chip MCM
- Substrate interconnect
- Low/med density D2D
- > 10um line/space
- > 125um bump pitch
- > 50um D2D spacing
- Chip last process

FanOut/RDL
- RDL interconnect
- Med/high density D2D
- > 1um line/space
- > 40um bump pitch
- > 100um D2D spacing
- Chip first/last
- FC to organic subs.
- No TSV – lower loss

2.5D TSV
- Si interconnect
- High density D2D
- < 0.5um line/space
- > 40um bump pitch
- > 50um D2D spacing
- Chip first/last
- High bandwidth
- Added Si layer
- Power limited

3D IC
- Si interconnect
- High density D2D
- Foundry line/space
- < 10um bump pitch
- High bandwidth
- Shortest interconnect
- Direct or hybrid bond
- Custom die designs

Increasing Bandwidth & Cost
Flip Chip / MCM

- Substrate based interconnect, > 10/10um line/space
- Multi-layer routing – 2/4 lyr core with build up layers
- Low to medium interconnect density (100’s to 1,000)
- Package size: < 80x80mm (prod), < 120x120mm (dev)
- D2D spacing capability: 60um

Benefits
- Supports homo/heterogenous die partitioning
- Enables IP reuse with advanced wafer node devices
- Reduced SoC design and validation time
- Enable multiple sources for ‘standard’ IP blocks / devices
- Smaller SoC die size – increased yield
- Lower bump/die stress – increased reliability

SoC + 16 chiplets
60um die to die spacing min
FanOut / FOCoS

- RDL based interconnect, 2/2um line/space
- Multi-layer routing (3-4 lys.)
- Medium to high interconnect density (1000’s to 10,000)
- Large FO area (1200-1600mm²)
- Stacked vias (10um hole/15um land)
- Chip first or chip last process

Benefits
- Die size, yield and cost optimization
- Process node / functionality optimization
- Integration of digital/analog SoCs
- Short, high density interconnect
- No TSV - Lower cost alternative to 2.5D
- Increased reliability vs. MCM
FOCoS Chip First Production Cross Sections
2.5D TSV Replacement Opportunity

2.5D Interposer Package

Fan Out Chip on Substrate 2.xD Package
FOCoS Chip Last With HBM

- Chip Last Construction
- 3,496 RDL traces to HBMs
- >15,500 C4 Bumps on Fan Out Composite Die
- 6 Metal Layers
  - 4 RDL layers
  - 2 layers with 2µm/2µm L/S
  - 1 UBM Layer
  - 1 C4 Layer
2.5D TSV

- Silicon based interconnect, < 0.5/0.5um line/space
- High interconnect density (10,000’s to 100,000)
- > 40um microbump pitch

Supports:
- Die partitioning
- Memory integration
- Optics integration (optical bench)

Benefits
- Silicon interconnect performance
- High bandwidth interface enablement
- Reduced power
- Si on Si first level interconnect
- System board size reduction
ASE - ODSA Engagement Objectives

• Respond to increased need for heterogeneous die integration
  • Disaggregation of complex die
  • Shrink system board into package
• Drive cost reduction & scaling
  • Reduce design & development time
  • Decrease customization
  • Engage supply chain
• Enable mass adoption
  • Develop package level interface design guidelines
  • Establish interface design libraries
  • Enable design & simulation tool integration

Open interface for chiplet communication
Next Steps / Call to Action

- Establish working group under/as part of ODSA CDX to focus on package interface design rules & layout
- Members to include:
  - ODSA BoW & OpenHBI interface architecture developers
  - Other / 3rd party interface architecture developers (AIB, XSR/USR, etc.)
  - EDA tool & library suppliers
  - Package substrate design/simulation service providers (OSAT and/or independent)
- Assess feasibility of establishing physical interface layout / pin out standards (eg. DDRx, HBM, AIB)
- Identify critical interface layout requirements and develop ‘PRD’ specification per interface
- Establish design guidelines and develop interface design libraries
  - Organic substrate interconnect (> 10um line/space)
  - Redistribution layer interconnect (> 1um line/space)
  - Silicon substrate (2.5D) interconnect (< 0.5um line/space)
- Demonstrate virtual chiplet integration design flow
Thank You

www.aseglobal.com