OCP CLB
Impedance Analysis

Ricky Lai
Hewlett Packard Enterprise
TDR - OCP CLB RX00
TDR - OCP CLB TX00
TDR – PCIe G4 CLB RX00
TDR – PCIe G4 CLB TX00
Why there is BIG impedance drop on OCP CLB?
### OCP CLB Stackup

- Cross section information from the board file

```
<table>
<thead>
<tr>
<th>Subclass Name</th>
<th>Type</th>
<th>Material</th>
<th>Thickness (MIL)</th>
<th>Tol +</th>
<th>Tol -</th>
<th>Conductivity (mho/cm)</th>
<th>Dielectric Constant</th>
<th>Loss Tangent</th>
</tr>
</thead>
<tbody>
<tr>
<td>SURFACE</td>
<td>CONDUCTOR</td>
<td>COPPER</td>
<td>1.900000</td>
<td>0</td>
<td>0</td>
<td>595900</td>
<td>4.5</td>
<td>0</td>
</tr>
<tr>
<td>TOP</td>
<td>CONDUCTOR</td>
<td>COPPER</td>
<td>1.900000</td>
<td>0</td>
<td>0</td>
<td>595900</td>
<td>4.5</td>
<td>0</td>
</tr>
<tr>
<td>TOP</td>
<td>DIELECTRIC</td>
<td>FR-4</td>
<td>2.700000</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>4.5</td>
<td>0.035</td>
</tr>
<tr>
<td>GND</td>
<td>PLANE</td>
<td>COPPER</td>
<td>1.300000</td>
<td>0</td>
<td>0</td>
<td>595900</td>
<td>4.5</td>
<td>0.035</td>
</tr>
<tr>
<td>GND</td>
<td>DIELECTRIC</td>
<td>FR-4</td>
<td>21.000000</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>4.5</td>
<td>0.035</td>
</tr>
<tr>
<td>VCC</td>
<td>PLANE</td>
<td>COPPER</td>
<td>1.300000</td>
<td>0</td>
<td>0</td>
<td>595900</td>
<td>4.5</td>
<td>0.035</td>
</tr>
<tr>
<td>VCC</td>
<td>DIELECTRIC</td>
<td>FR-4</td>
<td>5.600000</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>4.5</td>
<td>0.035</td>
</tr>
<tr>
<td>GD2</td>
<td>PLANE</td>
<td>COPPER</td>
<td>1.300000</td>
<td>0</td>
<td>0</td>
<td>595900</td>
<td>4.5</td>
<td>0.035</td>
</tr>
<tr>
<td>GD2</td>
<td>DIELECTRIC</td>
<td>FR-4</td>
<td>21.000000</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>4.5</td>
<td>0.035</td>
</tr>
<tr>
<td>GD3</td>
<td>PLANE</td>
<td>COPPER</td>
<td>1.300000</td>
<td>0</td>
<td>0</td>
<td>595900</td>
<td>4.5</td>
<td>0.035</td>
</tr>
<tr>
<td>GD3</td>
<td>DIELECTRIC</td>
<td>FR-4</td>
<td>2.700000</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>4.5</td>
<td>0.035</td>
</tr>
<tr>
<td>BOTTOM</td>
<td>CONDUCTOR</td>
<td>COPPER</td>
<td>1.900000</td>
<td>0</td>
<td>0</td>
<td>595900</td>
<td>4.5</td>
<td>0</td>
</tr>
<tr>
<td>SURFACE</td>
<td>AIR</td>
<td></td>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

Total Thickness: 62 MIL
6.3.5.1 Test Fixture Requirements

A test fixture for connector S-parameter measurement must be designed and built to the following:

- The test fixture used for measuring S-parameters will comprise a baseboard and mating Add-in Card fabricated from the same PCB panel. The total thickness of the boards, measured across the Add-in Card edge fingers, must be **1.57 mm** (062 mil).
- The PCB test fixture must be an FR-4 based material, or of a lower loss material with a relative permittivity of 3.6 or greater. Dielectric loss factor is not specified.
- The test PCB must have a microstrip structure: the microstrip’s dielectric thickness or stackup are recommended to be approximately **0.102 mm** (4 mil).
- The interconnect traces on all boards must be routed uncoupled (single ended) where possible. Some method of mitigating fiber weave effects must be applied. This can include off-axis routing or board rotation on the PCB panel.
OCP vs PCIe CLB stackup

**OCP**

- L1 prepreg: 2.7
- L2 (0.5 oz Cu): 1.3
- Core: 21.0
- L3 (0.5 oz Cu): 1.3
- Prepreg: 5.6
- L4 (0.5 oz Cu): 1.3
- Core: 21.0
- L5 (1.0 oz Cu): 1.3
- Prepreg: 2.7
- L6: 1.9
- Total thickness: 62.0

**PCle**

- L1 prepreg: 4.0
- L2 (0.5 oz Cu): 1.3
- Core: 47.6
- L3 (1.0 oz Cu): 1.3
- Prepreg: 4.0
- L4: 1.9
- Total thickness: 62.0
PCI-SIG Gen4 CLB X-section
SMP Header

- 30 mil wide metal on the SMP header creates large capacitance from L2 and thus causes significant impedance drop
How does PCI-SIG CLB get around?

• Create void underneath the header on L2
OCP CLB – L1

16 x 47

6 mil trace
OCP CLB – L2 & L3
Impedance Simulation Results

L1
prepreg 1.9
L2 (0.5 oz Cu) 2.7
core 1.3
L3 (0.5 oz Cu) 21.0
prepreg 1.3
L4 (0.5 oz Cu) 5.6
core 21.0
L5 (1.0 oz Cu) 1.3
prepreg 1.3
L6 2.7

total thickness 62.0

13 impedance if L2 is reference
37 impedance if L3 is reference (void on L2)
40 impedance if L4 is reference (void on L2 & L3)
43 impedance if L5 is reference (void on L2, L3 & L4)
Recommendation

• Create void underneath the SMP header on L2, L3 & L4