Programmable PON FPGA Design

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Sumithra Bhojan
Principal Member of Tech Staff
AT&T
Use of FPGA in OCP Telco

Engagement with FPGA and IP core providers
Business model similar to ASIC
Standard IP core made available for an OCP Spec
Option to customize for Operator requirements
Spec under development for Programmable PON (10G and 25G)
Programmable PON OLT

Design OLT spec for XGSPON; hardware capable of 25G PON upgrade in future
OLT port density of 24 for 1RU

What is desired from Operators?
- 19” 1 RU OLT design
- Open Sled design for CG-OpenRack-19
Programmable PON OLT

Partnering with Xilinx and Feneck
Build FPGA modules for PON MAC
(8) 10G ports per FPGA design
No aggregation in the OLT
Optional CPU
BMC Support
Block Diagram

FANS
PSU
BMC

Timing Block (optional)

COM Express Type 7 (optional)

10G/25G Octal PON FPGA #1
8x XFP (Any PON) 2x QSP28 Uplink

10G/25G Octal PON FPGA #2
8x XFP (Any PON) 2x QSP28 Uplink

10G/25G Octal PON FPGA #3
8x XFP (Any PON) 2x QSP28 Uplink

PCIe

100GE, 50GE, 40GE, 4x25GE, 8x10GE
XGS-PON, NG-PON2, 10GE-PON, 25G-PON

OPEN. FOR BUSINESS.
Open Access Architecture

Open Source Access Manager (OSAM)
Vendor agnostic operation interface for managing consumer broadband devices and services
Integrated to the ONAP framework
Domain Specific Controller (DSC)
Disaggregation of control and management plane
Hardware abstraction (VOLTHA/OSAM-HA)
Abstract and harmonize hardware interfaces and data

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G.fast Specification
- 16 port DPU-Broadcom Spec
- 16 port DPU-Sckipio Spec
16 port DPU-Broadcom Spec

- Coax and twisted pair
- Reverse power feed
- Uplink- 1G, 2.5G, 10G Ethernet or GPON/XGSPON
16 port DPU-Sckipio Spec

- Updated NPU – PRX321
- Coax and twisted pair
- Reverse power feed
- Uplink- 1G, 2.5G, 10G Ethernet or GPON/XGSPON
Call to Action

Collaboration/feedback to define detailed spec for Programmable PON OLT, FDH

Review of Spec - 16 port DPU-Sckipio v2.0, 16 port DPU-Broadcom v2.0