Using FPGA in OCP Specs

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Let’s talk FPGA!

Part of a Spectrum
CPLD – FPGA
Programmed in HDL,
Burned or loaded with a bit stream

Novel Opportunities
Processor cores, DSP cores, Memory, Mixed-Signal
Part of SoC compositions

How to treat FPGAs?
For CPLDs OCP typically expects the configuration or programming of CPLDs to be released with the OCP Spec
FPGAs are potentially much more complex – and often the programming (IP Core) is purchased or licensed
The licensing for FPGA IP Cores often looks like the licensing for merchant silicon programming libraries
Obviously, it is most preferred if FPGA IP Cores were opened and made available with an OCP spec in HDL
And perhaps just as obvious, if the FPGA were not available under any circumstances, then the OCP spec would not be useful as a publication
So, is there a middle ground where the FPGA IP must be made available, but under reasonable and non-discriminatory terms?
What is reasonable and non-discriminatory?